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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/842,482	04/25/2001	Gary B. Gordon	10980523-1	9824

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IP Administration
Legal Department, 20BN
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EXAMINER	
EPPERSON, JON D	
ART UNIT	**PAPER NUMBER**
1639	

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/842,482	GORDON ET AL.	
	Examiner	Art Unit	
	Jon D Epperson	1639	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *33-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *33-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Application

1. The Response filed January 9, 2004 is acknowledged.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Status of the Claims

3. Claims 33-35 were pending. Applicants amended claims 33-35. No claims were added or canceled. Therefore, claims 33-35 are currently pending and examined on the merits.

Withdrawn Objections/Rejections

4. The Montgomery/Bassous rejection under 35 U.S.C. 103(a) is withdrawn with respect to claims 33-34 in view of Applicants' amendments and/or arguments. All other rejections are maintained and the arguments are addressed below.

Outstanding Objections and/or Rejections

5. Claims 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Montgomery (US 6,093,302) in view of Bassous et al. (US 4,047,184) and the statements in the instant specification on page 22, lines 21-29.

The following analysis is used for this rejection:

Claim 33 is directed to a "method of fabricating a plurality of individual chips for conducting chemical reactions". The claim goes on to recite in step (a) "each site for

electronically carrying out a chemical reaction". Similarly, claim 34 is directed to a "method of fabricating a plurality of individual chips for conducting a part of a synthesis of oligonucleotides" reciting in step (a) "each site for electronically carrying out a part of a synthesis of oligonucleotides"; and claim 35 is directed to a "method of fabricating a plurality of individual chips for conducting a synthesis of oligonucleotides to form oligonucleotide arrays" reciting in step (a) "each site for electronically carrying out a synthesis of an oligonucleotide to form oligonucleotide arrays". The methods of the claims, however, comprise just two steps – "(a) preparing a plurality of said chips on a single silicon substrate...", and "(b) severing said single silicon substrate into said individual chips". The limitations in the preamble ("for conducting ...") and in step (a) ("for electronically carrying out ...") mentioned above are *intended use* recitations that merely recite the purpose of the process or the intended use of the structure and thus have not been accorded any patentable weight.

See MPEP 2111.02: A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976); and *Kropa v. Robie*, 187 F.2d at 152, 88 USPQ at 481. Also, "[i]n a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art." *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967); *In re Otto*, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963). Thus, the recitations in each of the claims described above (in the

preamble "for conducting ..." and in step (a) "for electronically carrying out ...") have not been given any patentable weight.

However, note that the primary reference used in this rejection (i.e. Montgomery) does deal with the synthesis of arrays of chemical polymers, e.g. nucleic acid sequences; see Abstract.

Montgomery teaches a method for electrochemical solid phase synthesis utilizing an array of electrodes (see patented claims 15 & 40). The electrode arrays of Montgomery are fabricated on a single silicon substrate using standard VLSI techniques and CMOS circuitry that is well known in the art. Specifically see column 31, line 46 – column 32, line 53; especially column 32, lines 14-21. The reference also teaches that the arrays can be any geometry and can contain electrodes of various sizes in various matrixes (see column 22, lines 17-52). Thus the electrode arrays of Montgomery read directly on the chips that are fabricated in the claimed methods.

Montgomery is silent as to the fabrication of more than one chip on a wafer (i.e. fabricating a plurality of chips) and the "severing" step. However, such a technique is very well-established in the art. For example, Bassous et al. teach creation of an electrode array and state that more than one array can be made on a single substrate where each electrode array chip is separated by scribing and dicing (see e.g. column 6, lines 34-37).

Moreover, applicants own specification states that art standard techniques of synthesis of the devices were utilized. See instant specification on page 22, lines 21-29:

the "devices used in the present invention may be fabricated according to procedures well-known to those skilled in the art of digital and IC design".

Lastly, it is noted that optimization of process steps is within the routine skill of the art. *In re Burhans*, 154 F.2d 690, 69 USPQ330 (CCPA 1946). Also, "[w]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA1955).

Therefore, it would have been *prima facie* obvious to one of ordinary skill in the art at the time of the invention to fabricate more than one of the devices (arrays of electrodes) of Montgomery; i.e. make more than one chip on a wafer and separate these chips via dicing. The general methodology of making multiple arrays on a single chip was well-known in the art as demonstrated by Bassous et al. and the instant specification. Thus applicants claims merely represent routine optimization. One of ordinary skill would have been motivated to create multiple chips for convenience in carrying out multiple experiments and for ease of manufacture. One of ordinary skill would also have had a reasonable expectation of success based on the fact that such fabrication procedures were well known and routine in the art at the time of filing.

Response

6. Applicant's arguments directed to the above 35 U.S.C. § 103(a) rejection were fully considered (and are incorporated in their entirety herein by reference) but were not deemed persuasive for the following reasons. Please note that the above rejection has been modified

from it original version to more clearly address applicants' newly amended and/or added claims and/or arguments.

Applicants argue, "There is nothing in the teaching of Montgomery or Bassous, or in the combined teachings, that would suggest dicing a substrate into individual chips after the synthesis of arrays of chemical compounds has been carried out on the surface of the substrate" (e.g., see 1/9/2004 Response, pages 4-6, especially page 6, paragraph 2).

This is not found persuasive for the following reasons:

The Examiner contends that Applicants' arguments are not commensurate in scope with the claimed invention. Due to the "comprising" language, the claim of course encompasses processes comprising these steps and any others. In addition, the recited steps need not even be carried out in the recited order. See *Interactive Gift Express, Inc. v. CompuServe Inc.*, 231 F.3d 859, 875, 56 USPQ2d 1647, 1661 (Fed. Cir. 2000) ("Unless the steps of a method actually recite an order, the steps are not ordinarily construed to require one."). Thus, Applicants contention that the chips must be diced "after" the synthesis of the arrays is without merit because Applicants' claims are not limited to this recited order.

Accordingly, the 35 U.S.C. § 103(a) rejection cited above is hereby maintained.

New Rejections

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Montgomery (US #6,093,302) and Bassous et al. (US #4,047,184) and if necessary Kobylecki et al. (US #6,153,375).

For ***claim 33-35***, Montgomery (see entire document) teaches (a) preparing on a silicon substrate an array of electronically addressable sites, each site for electronically carrying out a chemical reaction and each site comprising an electrode (e.g., see Montgomery, figure 5 wherein 5 addressable sites are shown for carrying out chemical reaction i.e., AA, AB, BA and BB monomers wherein each site comprises an electrode i.e., boxes 1-5; see also figure 10; see also patented claims 15 & 40). The electrode arrays of Montgomery are fabricated on a single silicon substrate using standard VLSI techniques and CMOS circuitry that is well known in the art (e.g., see column 31, line 46 – column 32, line 53; especially column 32, lines 14-21; see also column 22, lines 17-52).

Furthermore, Montgomery teaches applying reagents for synthesizing said chemical compounds on said substrate and utilizing said electronically addressable sites to conduct said synthesizing (e.g., see figures 5 and 10 wherein monomers are "applied" to synthesize chemical compounds i.e., the polymers; see also claim 15).

For ***claims 34-35***, Montgomery also teaches the use of nucleotide monomers for the synthesis of oligonucleotides (e.g., see example 2, especially column 30, paragraph 2).

The prior art teachings of Montgomery differ from the claimed invention as follows:

For ***claim 33-35***, Montgomery is silent as to the fabrication of more than one chip on a wafer (i.e. fabricating a plurality of chips) and "severing" said wafer "after" an array of chemical compounds (e.g., oligonucleotides) has been synthesized on said wafer.

However, Bassous et al. and if necessary Kobylecki et al. teach the following limitations that are deficient in Montgomery:

For ***claim 33-35***, Bassous et al. (see entire document) teach the creation of an electrode array and state that more than one array can be made on a single substrate where each electrode array chip is separated by scribing and dicing i.e., "severing" (see e.g. column 6, lines 34-37). Furthermore, Applicants have acknowledged that Bassous et al. teach severing said chip "before" the synthesis of the chemical compounds (e.g., see 1/9/2004 Response, "Montgomery and Bassous would yield a method wherein the substrate is diced into individual chips prior to the synthesis of compounds on its surface") as a preferred embodiment that leaves only one other possibility (i.e., slicing

"after" the synthesis) as an implicit less preferred teaching (e.g., see MPEP § 2123, "A reference may be relied upon for all that it would have reasonably suggested to one having ordinary skill the art, including nonpreferred embodiments. Merck & Co. v. Biocraft Laboratories, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989)").

Furthermore, it is noted that optimization of process steps is within the routine skill of the art. *In re Burhans*, 154 F.2d 690, 69 USPQ330 (CCPA 1946). Also, "[w]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA1955). Here, the Examiner contends that deciding when to "sever" the chip is within routine experimentation because there are only two possible alternatives (i.e., before or after the chemical synthesis) and the time at which the chip is severed has no material effect on the chip that is being synthesized (i.e., the same chip will be produced in either case). For example, Montgomery discloses compounds that are synthesized in a spatially addressable manner and, as a result, the inventor knows where to "sever" the chip regardless of whether the cutting is done before or after the synthesis.

For ***claims 33-35***, Kobylecki et al. (see entire document) further teach that chips can be severed "after" an array of chemical compounds has been synthesized thereon (e.g., see summary of the invention; see also figure 1; see especially claim 1 wherein the reference discusses further "subdividing" the parent chip after various stages of chemical synthesis).

Therefore, it would have been *prima facie* obvious to one of ordinary skill in the art at the time of the invention to fabricate more than one of the devices (arrays of electrodes) as taught by Montogomery via dicing as taught by Bassous et al. and if necessary Kobylecki et al. (i.e. to make more than one chip on a wafer and separate these chips "after" synthesis). The general methodology of making multiple arrays on a single chip was well-known in the art including separating said multiple arrays "after" synthesis as demonstrated by Bassous et al. and if necessary Kobylecki et al. Thus Applicants' claims merely represent routine optimization. One of ordinary skill would have been motivated to create multiple chips for convenience in carrying out multiple experiments and for ease of manufacture. Furthermore, Kobylecki et al. explicitly states that their method for manufacturing chips is "especially suitable for the preparation of natural and synthetic chemicals compounds" and also for "preparing combinatorial libraries", which would encompass the libraries of Montgomery. One of ordinary skill would also have had a reasonable expectation of success based on the fact that such fabrication procedures were well known and routine in the art at the time of filing and that Bassous clearly shows that these techniques can be applied to electrochemical chips.

Conclusion

Applicant's amendment necessitated any new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jon D Epperson whose telephone number is (571) 272-0808. The examiner can normally be reached Monday-Friday from 9:00 to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Wang can be reached on (571) 272-0811. The fax phone number for the organization where this application or proceeding is assigned is (571) 272-0811.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-1600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jon D. Epperson, Ph.D.
April 16, 2004

BENNETT CELSA
PRIMARY EXAMINER